an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths extending through said interposer from [one] said first surface to [the opposite] said second surface, forming electrical entry and exit ports on said insulating interposer;

said interposer positioned substantially parallel to the wafer [surface] having one of its surfaces attached to said [planar] conductive array, thereby electrically connecting said ports to at least some of said coupling members; and

a planar array of solder balls attached to said exit ports of said interposer.

Remarks

Favorable reconsideration and allowance of the application are respectfully requested in view of the above amendments and the following comments:

The rejection of claims 1-13 as unpatentable over Arima et al is respectfully traversed, since the reference fails to disclose or suggest the subject matter of applicant's claims. Note particularly that Arima is directed to the assembly of separate chips, whereas applicant's invention is directed to the assembly of a semiconductor wafer comprising a plurality of undivided chips, while the chips are still joined together by semiconductor crystal.

This is a huge difference. Clearly it is not "obvious" to substitute a complete wafer of undivided chips in the Arima process, to replace the plurality of separate chips

assembled by Arima et al. The concepts are worlds apart, since the purpose of applicant's invention is to provide a wafer scale assembly, which is subsequently divided into a multiplicity of single chips that are already packaged before dicing the wafer.

Thus the rejection is improper and should be withdrawn.

Respectfully submitted,

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